

# Le7920

## Subscriber Line Interface Circuit VE580 Series

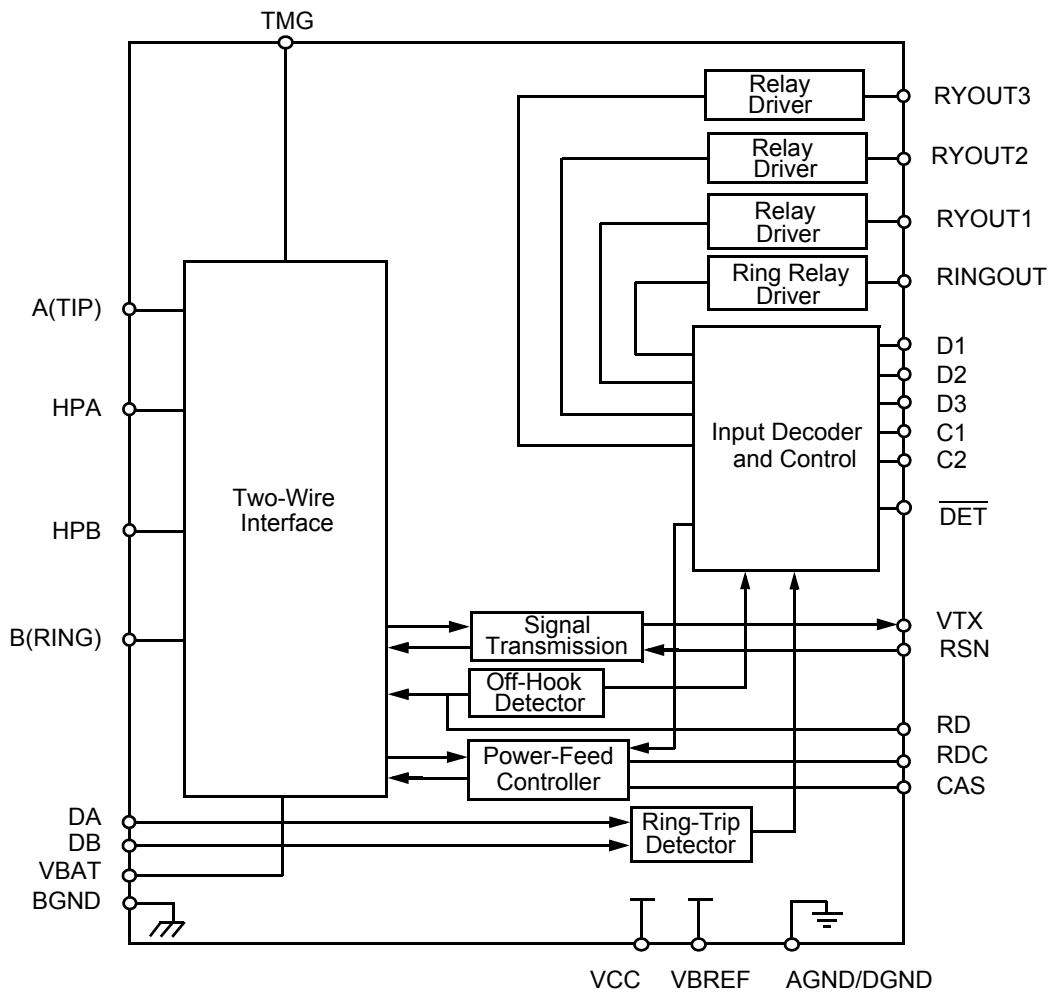
The Le7920 Subscriber Line Interface Circuit implements the basic telephone line interface functions, and enables the

design of low cost, high performance, POTS line interface cards.

### DISTINCTIVE CHARACTERISTICS

- Control states: Active, Ringing, Standby, and Disconnect
- Low standby power (35 mW)
- -19 V to -58 V battery operation
- On-hook transmission
- Two-wire impedance set by single external impedance
- Programmable constant-current feed
- Programmable loop-detect threshold
- Programmable ring-trip detect threshold
- No -5 V supply required
- Current Gain = 500
- On-chip Thermal Management (TMG) feature
- Four on-chip relay drivers and relay snubbers, 1 ringing and 3 general purpose (32 PLCC)

### BLOCK DIAGRAM



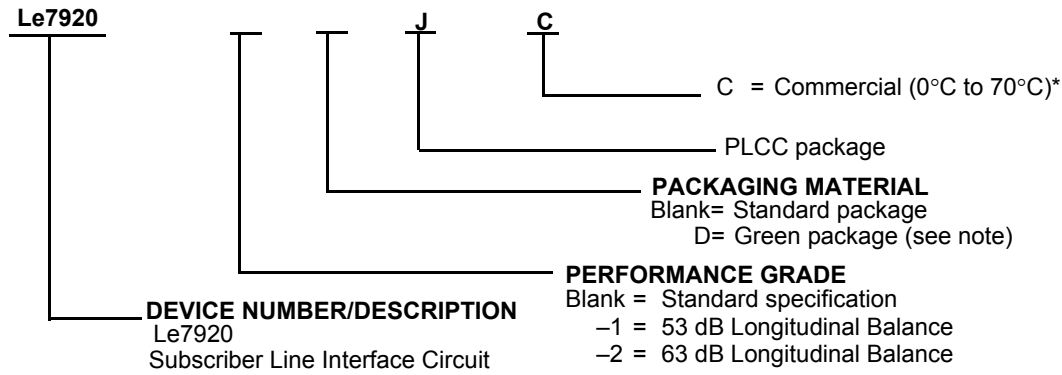
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## ORDERING INFORMATION

### Standard Products

Zarlink standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



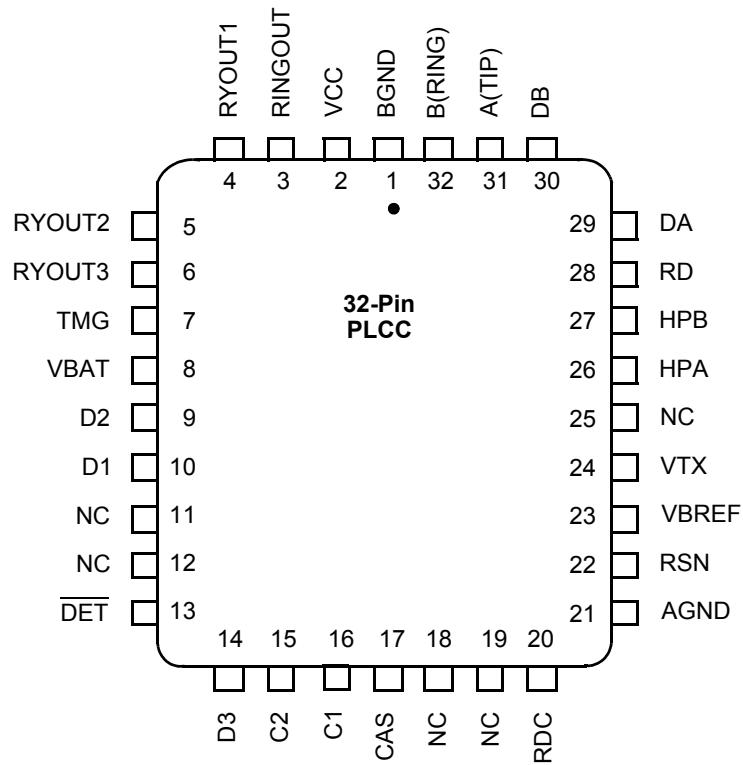
**Note:** Green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Zarlink sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Zarlink's standard military-grade products.

| Valid Combinations |    |     |
|--------------------|----|-----|
| Le7920*            | -1 | JC  |
|                    | -2 | DJC |

*\*Zarlink reserves the right to fulfill all orders for this device with parts marked with the "Am" part number prefix, until such time as all inventory bearing this mark has been depleted. It should be noted that parts marked with either the "Am" or the "Le" part number prefix are equivalent devices in terms of form, fit, and function. The only difference between the two is in the part number prefix appearing on the topside mark.*

**CONNECTION DIAGRAM****Top View****Notes:**

1. Pin 1 is marked for orientation.
2. NC = No Connect

**PIN DESCRIPTIONS**

| Pin Name  | Type      | Description                                                                                                                                                                                                                                                |
|-----------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AGND/DGND | Ground    | Analog and Digital ground.                                                                                                                                                                                                                                 |
| A(TIP)    | Output    | Output of A(TIP) power amplifier.                                                                                                                                                                                                                          |
| BGND      | Ground    | Battery (power) ground.                                                                                                                                                                                                                                    |
| B(RING)   | Output    | Output of B(RING) power amplifier.                                                                                                                                                                                                                         |
| C2–C1     | Inputs    | Decoder. TTL compatible. C2 is MSB and C1 is LSB.                                                                                                                                                                                                          |
| CAS       | Capacitor | Anti-Saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.                                                                                                                                                    |
| D3–D1     | Input     | Relay Driver Control. D3–D1 control the relay drivers RYOUT1, RYOUT2, and RYOUT3. Logic Low on D1 activates the RYOUT1 relay driver. Logic Low on D2 activates the RYOUT2 relay driver. Logic Low on D3 activates the RYOUT3 relay driver. TTL compatible. |
| DA        | Input     | Ring-trip negative. Negative input to ring-trip comparator.                                                                                                                                                                                                |
| DB        | Input     | Ring-trip positive. Positive input to ring-trip comparator.                                                                                                                                                                                                |
| DET       | Output    | Switchhook detector. Logic Low indicates that selected detector is tripped. Logic inputs C2–C1, E1, and E0 select the detector. Open-collector with a built-in 15 k $\Omega$ pull-up resistor.                                                             |
| HPA       | Capacitor | High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.                                                                                                                                                                                     |
| HPB       | Capacitor | High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.                                                                                                                                                                                    |
| NC        | —         | No Connect. Pin not internally connected.                                                                                                                                                                                                                  |
| RD        | Resistor  | Detect resistor. Detector threshold set and filter pin.                                                                                                                                                                                                    |
| RDC       | Resistor  | DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN).                                                                                                  |
| RINGOUT   | Output    | Ring Relay Driver. Open-collector driver with emitter internally connected to BGND.                                                                                                                                                                        |
| RSN       | Input     | Receive Summing Node. The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 500 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node.          |
| RYOUT1    | Output    | Relay/Switch Driver. Open-collector driver with emitter internally connected to BGND.                                                                                                                                                                      |
| RYOUT2    | Output    | Relay/Switch Driver. Open-collector driver with emitter internally connected to BGND (PLCC only).                                                                                                                                                          |
| RYOUT3    | Output    | Relay/Switch Driver. Open-collector driver with emitter internally connected to BGND (PLCC only).                                                                                                                                                          |
| TMG       | —         | Thermal Management. External resistor connects between this pin and VBAT to offload power from SLIC.                                                                                                                                                       |
| VBAT      | Battery   | Battery supply and connection to substrate.                                                                                                                                                                                                                |
| VBREF     | —         | This is an Zarlink reserved pin and must always be connected to the VBAT pin.                                                                                                                                                                              |
| VCC       | Power     | +5 V power supply.                                                                                                                                                                                                                                         |
| VTX       | Output    | Transmit Audio. This output is a 0.50 gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.                                                                                          |

**ABSOLUTE MAXIMUM RATINGS**

Storage temperature .....  $-55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

$V_{\text{CC}}$  with respect to AGND/DGND .....  $-0.4\text{ V}$  to  $+7.0\text{ V}$

$V_{\text{BAT}}$  with respect to AGND/DGND:

Continuous .....  $+0.4\text{ V}$  to  $-70\text{ V}$

10 ms .....  $+0.4\text{ V}$  to  $-75\text{ V}$

BGND with respect to AGND/DGND .....  $+3\text{ V}$  to  $-3\text{ V}$

A(TIP) or B(RING) to BGND:

Continuous .....  $V_{\text{BAT}}$  to  $+1\text{ V}$

10 ms ( $f = 0.1\text{ Hz}$ ) .....  $-70\text{ V}$  to  $+5\text{ V}$

1  $\mu\text{s}$  ( $f = 0.1\text{ Hz}$ ) .....  $-80\text{ V}$  to  $+8\text{ V}$

250 ns ( $f = 0.1\text{ Hz}$ ) .....  $-90\text{ V}$  to  $+12\text{ V}$

Current from A(TIP) or B(RING) .....  $\pm 150\text{ mA}$

RINGOUT/RYOUT1,2,3 current .....  $50\text{ mA}$

RINGOUT/RYOUT1,2,3 voltage ..... BGND to  $+7\text{ V}$

RINGOUT/RYOUT1,2,3 transient ..... BGND to  $+10\text{ V}$

DA and DB inputs

Voltage on ring-trip inputs .....  $V_{\text{BAT}}$  to  $0\text{ V}$

Current into ring-trip inputs .....  $\pm 10\text{ mA}$

C2–C1 and D3–D1

Input voltage .....  $-0.4\text{ V}$  to  $V_{\text{CC}} + 0.4\text{ V}$

Maximum power dissipation, continuous,

$T_{\text{A}} = 70^{\circ}\text{C}$ , No heat sink (See note)

In 32-pin PLCC package .....  $1.7\text{ W}$

Thermal Data: .....  $\theta_{\text{JA}}$

In 32-pin PLCC package .....  $43^{\circ}\text{C/W typ}$

ESD immunity/pin (HBM) .....  $1500\text{ V}$

**Note:** Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about  $165^{\circ}\text{C}$ . Continuous operation above  $145^{\circ}\text{C}$  junction temperature may degrade device reliability.

Stresses above those listed under "Absolute Maximum Ratings" can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

The operating ranges define those limits between which the functionality of the device is guaranteed.

### Commercial (C) Devices

Ambient temperature .....0°C to +70°C\*

V<sub>CC</sub>..... 4.75 V to 5.25 V

V<sub>BAT</sub>..... –19 V to –58 V

AGND/DGND ..... 0 V

BGND with respect to

AGND/DGND ..... –100 mV to +100 mV

Load resistance on VTX to ground ..... 20 kΩ min

*\* Zarlink guarantees the performance of this device over commercial (0 to 70°C) and industrial (–40 to 85°C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.*

### Package Assembly

The standard (non-green) package devices are assembled with industry-standard mold compounds, and the leads possess a tin/lead (Sn/Pb) plating. These packages are compatible with conventional SnPb eutectic solder board assembly processes. The peak soldering temperature should not exceed 225°C during printed circuit board assembly.

The green package devices are assembled with enhanced environmental compatible lead (Pb), halogen, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile

**ELECTRICAL CHARACTERISTICS**

| Description                                                          | Test Conditions (See Note 1)                                                 | Min            | Typ        | Max            | Unit  | Note   |
|----------------------------------------------------------------------|------------------------------------------------------------------------------|----------------|------------|----------------|-------|--------|
| Transmission Performance                                             |                                                                              |                |            |                |       |        |
| 2-wire return loss                                                   | 200 Hz to 3.4 kHz                                                            | 26             |            |                | dB    | 1, 4   |
| Analog output (VTX) impedance                                        |                                                                              |                | 3          | 20             | Ω     | 4      |
| Analog (VTX) output offset voltage                                   |                                                                              | −50            |            | +50            | mV    |        |
| Overload level, 2-wire and 4-wire                                    | Active state                                                                 | 2.5            |            |                | Vpk   | 2a     |
| Overload level                                                       | On hook, R <sub>LAC</sub> = 600 Ω                                            | 0.77           |            |                | Vrms  | 2b     |
| THD, Total Harmonic Distortion                                       | 0 dBm<br>+7 dBm                                                              |                | −64<br>−55 | −50<br>−40     | dB    | 5      |
| THD, On hook                                                         | 0 dBm, R <sub>LAC</sub> = 600 Ω                                              |                |            | −36            |       |        |
| Longitudinal Capability (See Test Circuit D)                         |                                                                              |                |            |                |       |        |
| Longitudinal to metallic L-T, L-4 balance                            | 200 Hz to 1 kHz                                                              |                |            |                | dB    | 4<br>4 |
|                                                                      | 0°C to +70°C −1*                                                             | 52             |            |                |       |        |
|                                                                      | 0°C to +70°C −2                                                              | 63             |            |                |       |        |
|                                                                      | −40°C to +85°C −1                                                            | 50             |            |                |       |        |
|                                                                      | −40°C to +85°C −2                                                            | 58             |            |                |       | 4<br>4 |
|                                                                      | 1 kHz to 3.4 kHz                                                             |                |            |                |       |        |
|                                                                      | 0°C to +70°C −1*                                                             | 52             |            |                |       |        |
|                                                                      | 0°C to +70°C −2                                                              | 58             |            |                |       |        |
|                                                                      | −40°C to +85°C −1                                                            | 50             |            |                |       |        |
|                                                                      | −40°C to +85°C −2                                                            | 53             |            |                |       |        |
| Longitudinal signal generation 4-L                                   | 200 Hz to 3.4 kHz                                                            | 40             |            |                |       |        |
| Longitudinal current per pin (A or B)                                | Active state                                                                 | 20             | 27         | 35             | mArms | 8      |
| Longitudinal impedance at A or B                                     | 0 to 100 Hz                                                                  |                | 25         |                | Ω/pin |        |
| Idle Channel Noise                                                   |                                                                              |                |            |                |       |        |
| C-message weighted noise                                             | R <sub>L</sub> = 600 Ω 0°C to +70°C<br>R <sub>L</sub> = 600 Ω −40°C to +85°C |                | 7          | +10<br>+12     | dBrnc | 4      |
| Psophometric weighted noise                                          | R <sub>L</sub> = 600 Ω 0°C to +70°C<br>R <sub>L</sub> = 600 Ω −40°C to +85°C |                | −83        | −80<br>−78     | dBmp  |        |
| Insertion Loss and Balance Return Signal (See Test Circuits A and B) |                                                                              |                |            |                |       |        |
| Gain accuracy 4- to 2-wire                                           | 0 dBm, 1 kHz                                                                 | −0.20          | 0          | +0.20          | dB    | 4      |
| Gain accuracy 2- to 4-wire, 4- to 4-wire                             | 0 dBm, 1 kHz                                                                 | −6.22          | −6.02      | −5.82          |       |        |
| Gain accuracy, 4- to 2-wire                                          | On hook                                                                      | −0.35          |            | +0.35          |       |        |
| Gain accuracy, 2- to 4-wire, 4- to 4-wire                            | On hook                                                                      | −6.37          | −6.02      | −5.67          |       |        |
| Gain accuracy over frequency                                         | 300 to 3.4 kHz relative to 1 kHz                                             | −0.15          |            | +0.15          |       |        |
| Gain tracking                                                        | +3 dBm to −55 dBm relative to 0 dBm                                          | −0.15          |            | +0.15          |       |        |
| Gain tracking On hook                                                | 0 dBm to −37 dBm<br>+3 dBm to 0 dBm                                          | −0.15<br>−0.35 |            | +0.15<br>+0.35 |       |        |
| Group delay                                                          | 0 dBm, 1 kHz                                                                 |                | 4          |                | μs    | 4, 7   |

**Note:**

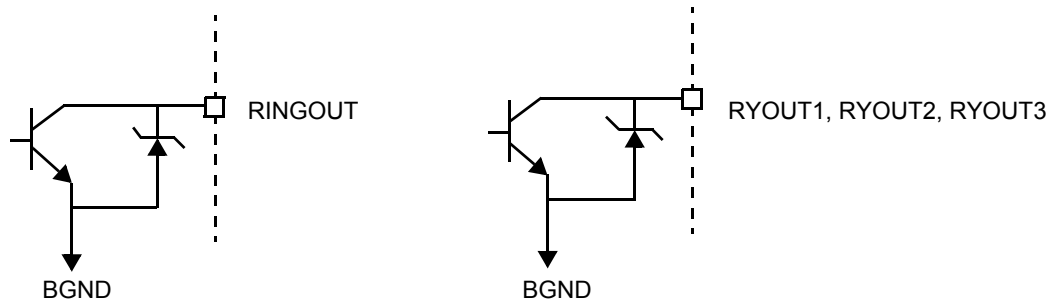
\* Performance Grade

**ELECTRICAL CHARACTERISTICS (continued)**

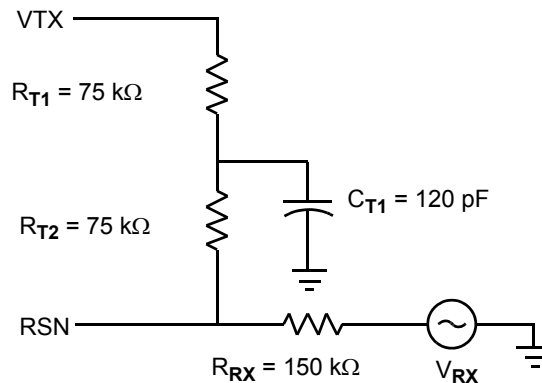
| Description                                                                          | Test Conditions (See Note 1)                                              | Min               | Typ            | Max               | Unit  | Note |
|--------------------------------------------------------------------------------------|---------------------------------------------------------------------------|-------------------|----------------|-------------------|-------|------|
| Line Characteristics                                                                 |                                                                           |                   |                |                   |       |      |
| I <sub>L</sub> , Short Loops, Active state                                           | R <sub>LDC</sub> = 600 Ω                                                  | 20                | 23             | 26                | mA    |      |
| I <sub>L</sub> , Long Loops, Active state                                            | R <sub>LDC</sub> = 1930 Ω, BAT = −42.75 V, T <sub>A</sub> = 25°C          | 18                | 19             |                   |       |      |
| I <sub>L</sub> , Accuracy, Standby state                                             | $I_L = \frac{ BAT  - 3\text{ V}}{R_L + 400} \quad T_A = 25^\circ\text{C}$ | 0.7I <sub>L</sub> | I <sub>L</sub> | 1.3I <sub>L</sub> |       |      |
|                                                                                      | Constant-current region                                                   | 18                | 30             |                   |       |      |
| I <sub>L</sub> , Loop current, Disconnect state                                      | R <sub>L</sub> = 0                                                        |                   |                | 100               | μA    |      |
| I <sub>L</sub> LIM                                                                   | Active, A and B to ground                                                 |                   | 85             | 120               | mA    |      |
| VAB, Open Circuit voltage                                                            | V <sub>BAT</sub> = −52 V                                                  | −42.75            | −44            |                   | V     |      |
| Power Supply Rejection Ratio (V <sub>RI</sub> PPLE = 100 mVrms), Active Normal State |                                                                           |                   |                |                   |       |      |
| V <sub>CC</sub>                                                                      | 50 Hz to 3.4 kHz                                                          | 30                | 40             |                   | dB    | 5    |
| V <sub>BAT</sub>                                                                     | 50 Hz to 3.4 kHz                                                          | 28                | 50             |                   |       |      |
| Effective internal resistance                                                        | CAS pin to V <sub>BAT</sub>                                               | 85                | 170            | 255               | kΩ    | 4    |
| Power Dissipation                                                                    |                                                                           |                   |                |                   |       |      |
| On hook, Disconnect state                                                            |                                                                           |                   | 25             | 70                | mW    |      |
| On hook, Standby state                                                               |                                                                           |                   | 35             | 100               |       |      |
| On hook, Active state                                                                |                                                                           |                   | 125            | 270               |       |      |
| Off hook, Standby state                                                              | R <sub>L</sub> = 600 Ω                                                    |                   | 860            | 1200              |       |      |
| Off hook, Active state                                                               | R <sub>L</sub> = 300 Ω, R <sub>T</sub> MG = 2350 Ω                        |                   | 450            | 800               |       |      |
| Supply Currents, Battery = −48V                                                      |                                                                           |                   |                |                   |       |      |
| I <sub>CC</sub> ,<br>On-hook V <sub>CC</sub> supply current                          | Disconnect state                                                          |                   | 1.7            | 4.0               | mA    |      |
|                                                                                      | Standby state                                                             |                   | 2.2            | 4.0               |       |      |
|                                                                                      | Active state, BAT = −48 V                                                 |                   | 6.3            | 8.5               |       |      |
| I <sub>BAT</sub> ,<br>On-hook V <sub>BAT</sub> supply current                        | Disconnect state                                                          |                   | 0.25           | 1.0               |       |      |
|                                                                                      | Standby state                                                             |                   | 0.55           | 1.5               |       |      |
|                                                                                      | Active state, BAT = −48 V                                                 |                   | 2.8            | 4.8               |       |      |
| RFI Rejection                                                                        |                                                                           |                   |                |                   |       |      |
| RFI rejection                                                                        | 100 kHz to 30 MHz, (See Figure F)                                         |                   |                | 1.0               | mVrms | 4    |
| Receive Summing Node (RSN)                                                           |                                                                           |                   |                |                   |       |      |
| RSN DC voltage                                                                       | I <sub>RSN</sub> = 0 mA                                                   |                   | 0              |                   | V     | 4    |
| RSN impedance                                                                        | 200 Hz to 3.4 kHz                                                         |                   | 10             | 20                | Ω     |      |
| Logic Inputs (C2–C1 and D3–D1)                                                       |                                                                           |                   |                |                   |       |      |
| V <sub>I</sub> H, Input High voltage                                                 |                                                                           | 2.0               |                |                   | V     |      |
| V <sub>I</sub> L, Input Low voltage                                                  |                                                                           |                   |                | 0.8               |       |      |
| I <sub>I</sub> H, Input High current                                                 |                                                                           | −75               |                | 40                | μA    |      |
| I <sub>I</sub> L, Input Low current                                                  |                                                                           | −400              |                |                   |       |      |
| Logic Output (DET)                                                                   |                                                                           |                   |                |                   |       |      |
| V <sub>O</sub> L, Output Low voltage                                                 | I <sub>O</sub> UT = 0.3 mA, 15 kΩ to V <sub>CC</sub>                      |                   |                | 0.40              | V     |      |
| V <sub>O</sub> H, Output High voltage                                                | I <sub>O</sub> UT = −0.1 mA, 15 kΩ to V <sub>CC</sub>                     | 2.4               |                |                   |       |      |
| Ring-Trip Detector Input (DA, DB)                                                    |                                                                           |                   |                |                   |       |      |
| Bias current                                                                         |                                                                           | −500              | −50            |                   | nA    |      |
| Offset voltage                                                                       | Source resistance = 2 MΩ                                                  | −50               | 0              | +50               | mV    | 6    |

**ELECTRICAL CHARACTERISTICS (continued)**

| Description                                           | Test Conditions (See Note 1) | Min  | Typ  | Max  | Unit | Note |
|-------------------------------------------------------|------------------------------|------|------|------|------|------|
| Loop Detector                                         |                              |      |      |      |      |      |
| On threshold                                          | R <sub>D</sub> = 35.4 kΩ     | 11.5 |      | 17.3 | mA   |      |
| Off threshold                                         | R <sub>D</sub> = 35.4 kΩ     | 9.4  |      | 14.1 |      |      |
| Hysteresis                                            | R <sub>D</sub> = 35.4 kΩ     | 0    |      | 4.4  |      |      |
| Relay Driver Output (RINGOUT, RYOUT1, RYOUT2, RYOUT3) |                              |      |      |      |      |      |
| On voltage                                            | I <sub>OL</sub> = 40 mA      |      | +0.3 | +0.7 | V    |      |
| Off leakage                                           | V <sub>OH</sub> = +5 V       |      |      | 100  | μA   |      |
| Zener breakover                                       | I <sub>Z</sub> = 100 μA      | 6    | 7.2  |      | V    |      |
| Zener On voltage                                      | I <sub>Z</sub> = 30 mA       |      | 10   |      |      |      |

**RELAY DRIVER SCHEMATICS****Notes:**

1. Unless otherwise noted, test conditions are  $BAT = -52 \text{ V}$ ,  $V_{CC} = +5 \text{ V}$ ,  $R_L = 600 \text{ }\Omega$ ,  $R_{DC1} = R_{DC2} = 27.17 \text{ k}\Omega$ ,  $R_{TMG} = 2350 \text{ }\Omega$ ,  $R_D = 35.4 \text{ k}\Omega$ , no fuse resistors,  $C_{HP} = 0.22 \text{ }\mu\text{F}$ ,  $C_{DC} = 0.1 \text{ }\mu\text{F}$ ,  $C_{CAS} = 0.33 \text{ }\mu\text{F}$ ,  $D1 = 1N400x$ , two-wire AC input impedance is a  $600 \text{ }\Omega$  resistance synthesized by the programming network shown below.



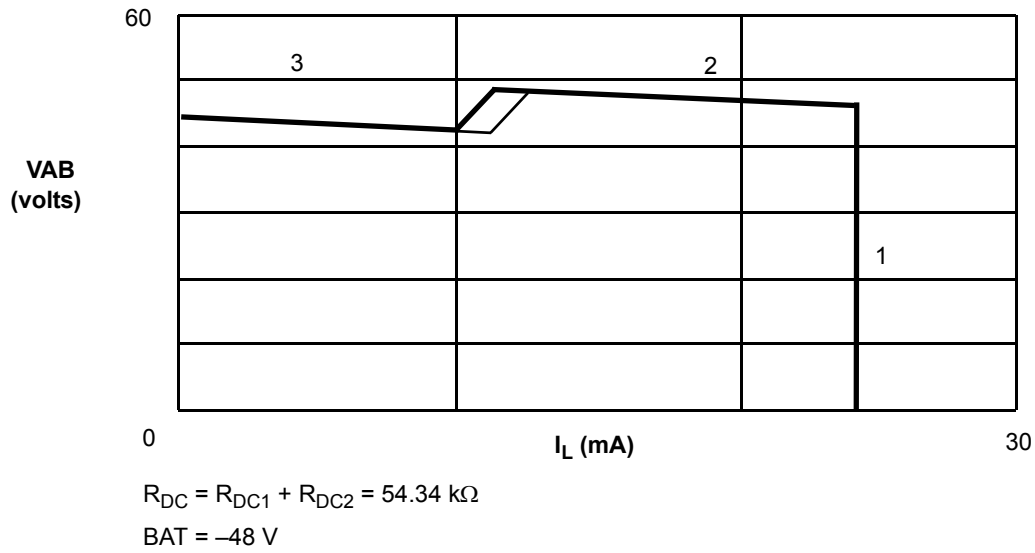
2. a. Overload level is defined when  $THD = 1\%$ .  
b. Overload level is defined when  $THD = 1.5\%$ .
3. Balance return signal is the signal generated at  $V_{TX}$  by  $V_{RX}$ . This specification assumes that the two-wire, AC-load impedance matches the programmed impedance.
4. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
5. This parameter is tested at  $1 \text{ kHz}$  in production. Performance at other frequencies is guaranteed by characterization.
6. Tested with  $0 \text{ }\Omega$  source impedance.  $2 \text{ M}\Omega$  is specified for system design only.
7. Group delay can be greatly reduced by using a  $Z_T$  network such as that shown in Note 1. The network reduces the group delay to less than  $2 \text{ }\mu\text{s}$  and increases  $2WRL$ . The effect of group delay on linecard performance also may be compensated for by synthesizing complex impedance with the QSLAC™ or DSLAC™ device.
8. Minimum current level guaranteed not to cause a false loop detect.

Table 1. SLIC Decoding

| State | C2 | C1 | Two-Wire Status | $\overline{\text{DET}}$ Output |
|-------|----|----|-----------------|--------------------------------|
| 0     | 0  | 0  | Disconnect      | Ring trip                      |
| 1     | 0  | 1  | Ringing         | Ring trip                      |
| 2     | 1  | 0  | Active          | Loop detector                  |
| 3     | 1  | 1  | Standby         | Loop detector                  |

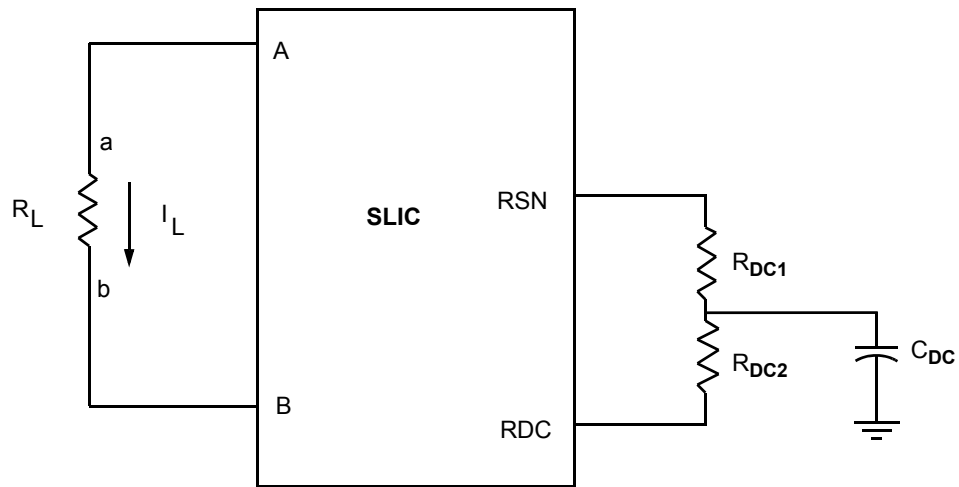
Table 2. User-Programmable Components

|                                                                                                                                |                                                                                                                                                                                                                                                                                        |
|--------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $Z_T = 250(Z_{2WIN} - 2R_F)$                                                                                                   | $Z_T$ is connected between the VTX and RSN pins. The fuse resistors are $R_F$ , and $Z_{2WIN}$ is the desired 2-wire AC input impedance. When computing $Z_T$ , the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account. |
| $Z_{RX} = \frac{Z_L}{G_{42L}} \cdot \frac{500Z_T}{Z_T + 250(Z_L + 2R_F)}$                                                      | $Z_{RX}$ is connected from VRX to RSN. $Z_T$ is defined above, and $G_{42L}$ is the desired receive gain.                                                                                                                                                                              |
| $R_{DC1} + R_{DC2} = \frac{1250}{I_{LOOP}}$<br>$C_{DC} = 1.5 \text{ ms} \cdot \frac{R_{DC1} + R_{DC2}}{R_{DC1} \cdot R_{DC2}}$ | $R_{DC1}$ , $R_{DC2}$ , and $C_{DC}$ form the network connected to the $R_{DC}$ pin. $R_{DC1}$ and $R_{DC2}$ are approximately equal. $I_{LOOP}$ is the desired loop current in the constant-current region.                                                                           |
| $R_{DON} = \frac{510}{I_T}$ , $R_{DOFF} = \frac{415}{I_T}$ , $C_D = \frac{0.5 \text{ ms}}{R_D}$                                | $R_D$ and $C_D$ form the network connected from $R_D$ to AGND/DGND and $I_T$ is the threshold current between on hook and off hook.                                                                                                                                                    |
| $C_{CAS} = \frac{1}{3.4 \cdot 10^5 \pi f_c}$                                                                                   | $C_{CAS}$ is the regulator filter capacitor and $f_c$ is the desired filter cut-off frequency.                                                                                                                                                                                         |
| $I_{STANDBY} = \frac{ V_{BAT}  - 3 \text{ V}}{400 \Omega + R_L}$                                                               | Standby loop current (resistive region).                                                                                                                                                                                                                                               |
| <b>Thermal Management Equations (Normal Active and Tip Open States)</b>                                                        |                                                                                                                                                                                                                                                                                        |
| $R_{TMG} \geq \left( \frac{ V_{BAT}  - 6 \text{ V}}{I_{LOOP}} - 70 \Omega \right)$                                             | $R_{TMG}$ is connected from TMG to VBAT and saves power within the SLIC in Active and Disconnect state constant-currents only.                                                                                                                                                         |
| $P_{RTMG} = \frac{( V_{BAT}  - 6 \text{ V} - (I_L \cdot R_L))^2}{(R_{TMG} + 70 \Omega)^2} \cdot R_{TMG}$                       | Power dissipated in the TMG resistor, $R_{TMG}$ , during Active and Disconnect states.                                                                                                                                                                                                 |
| $P_{SLIC} =  V_{BAT}  \cdot I_L - P_{RTMG} - R_L(I_L)^2 + 0.12 \text{ W}$                                                      | Power dissipated in the SLIC while in Active and Disconnect states.                                                                                                                                                                                                                    |

**DC FEED CHARACTERISTICS****Notes:**

1.  $V_{AB} = I_L R_L' = \frac{1250}{R_{DC}} R_L'$ , where  $R_L' = R_L + 2R_F$
2.  $V_{AB} = 0.857(|V_{BAT}| + 3.3) - I_L \frac{R_{DC}}{300}$
3.  $V_{AB} = 0.857(|V_{BAT}| + 1.2) - I_L \frac{R_{DC}}{300}$

**a. Load Line (Typical)**

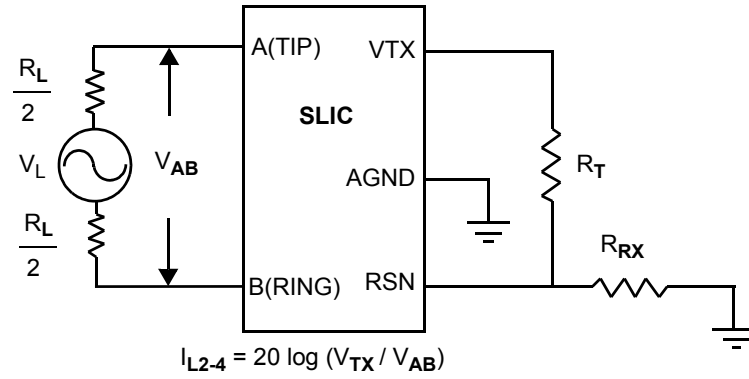
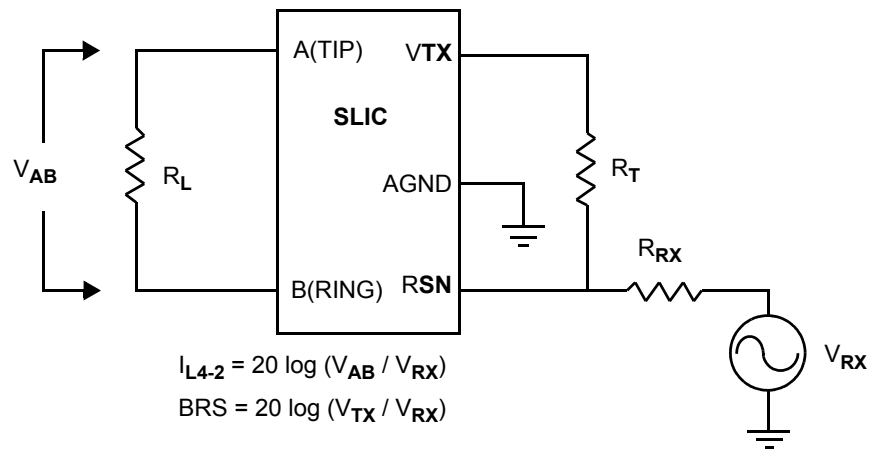
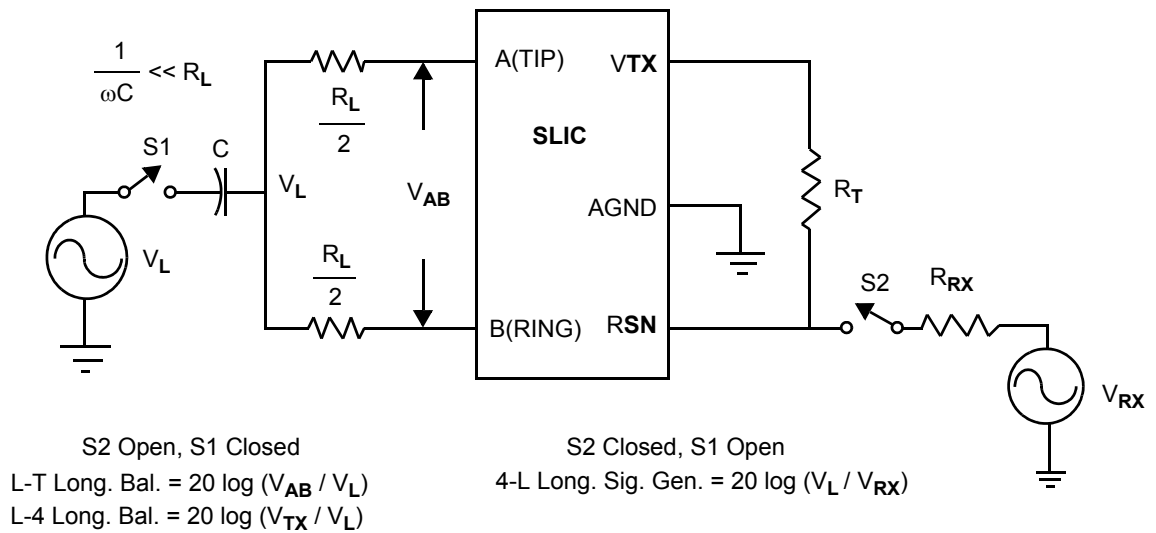


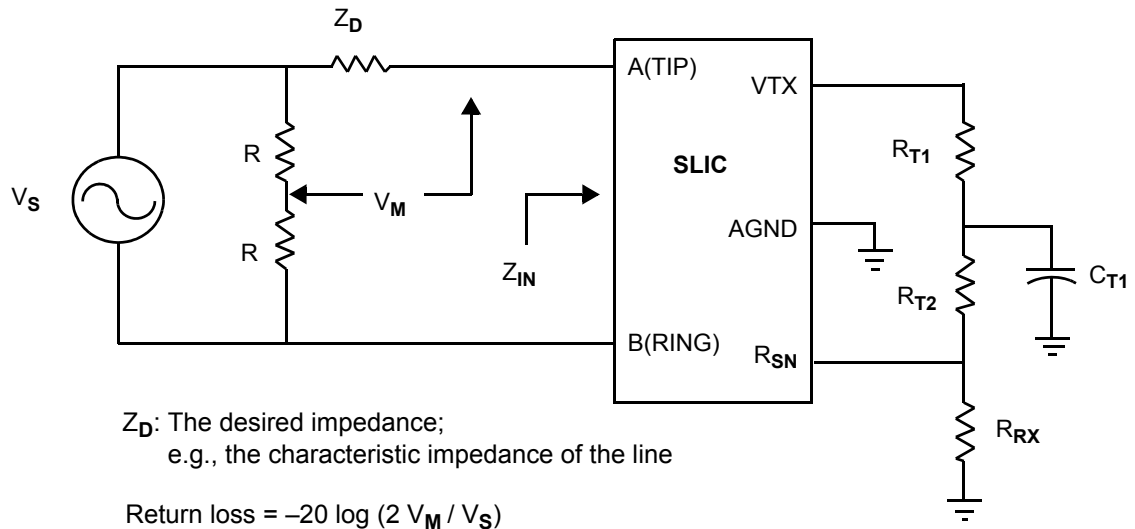
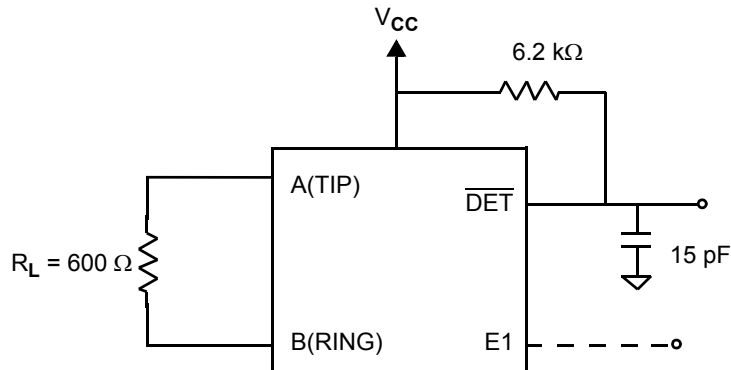
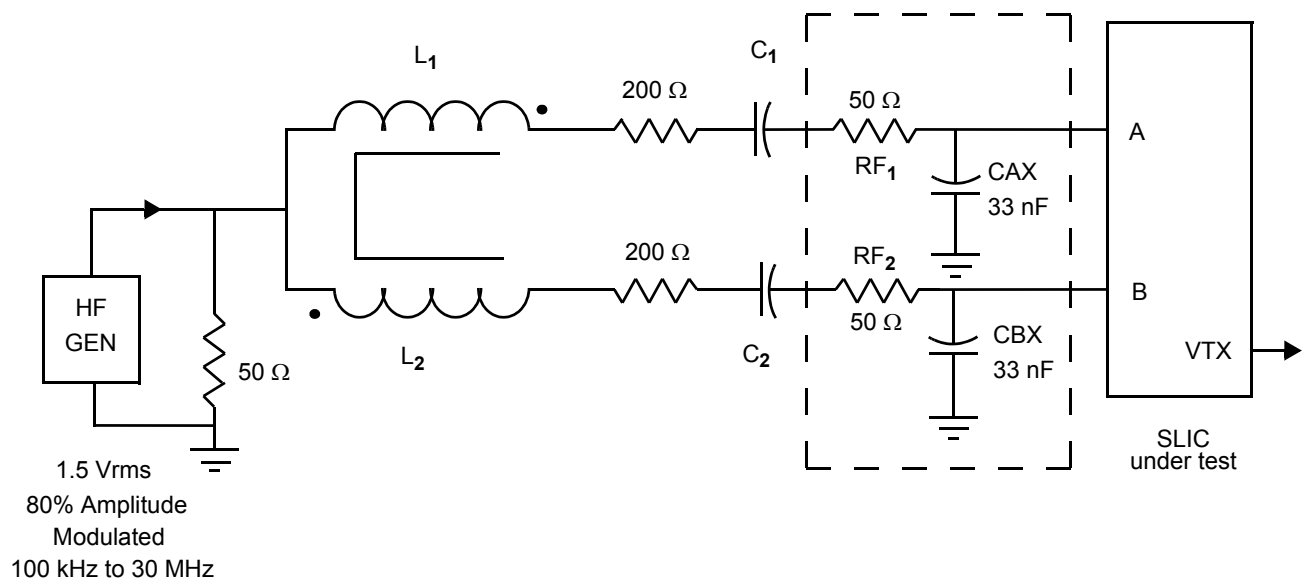
Feed current programmed by  $R_{DC1}$  and  $R_{DC2}$

#### b. Feed Programming

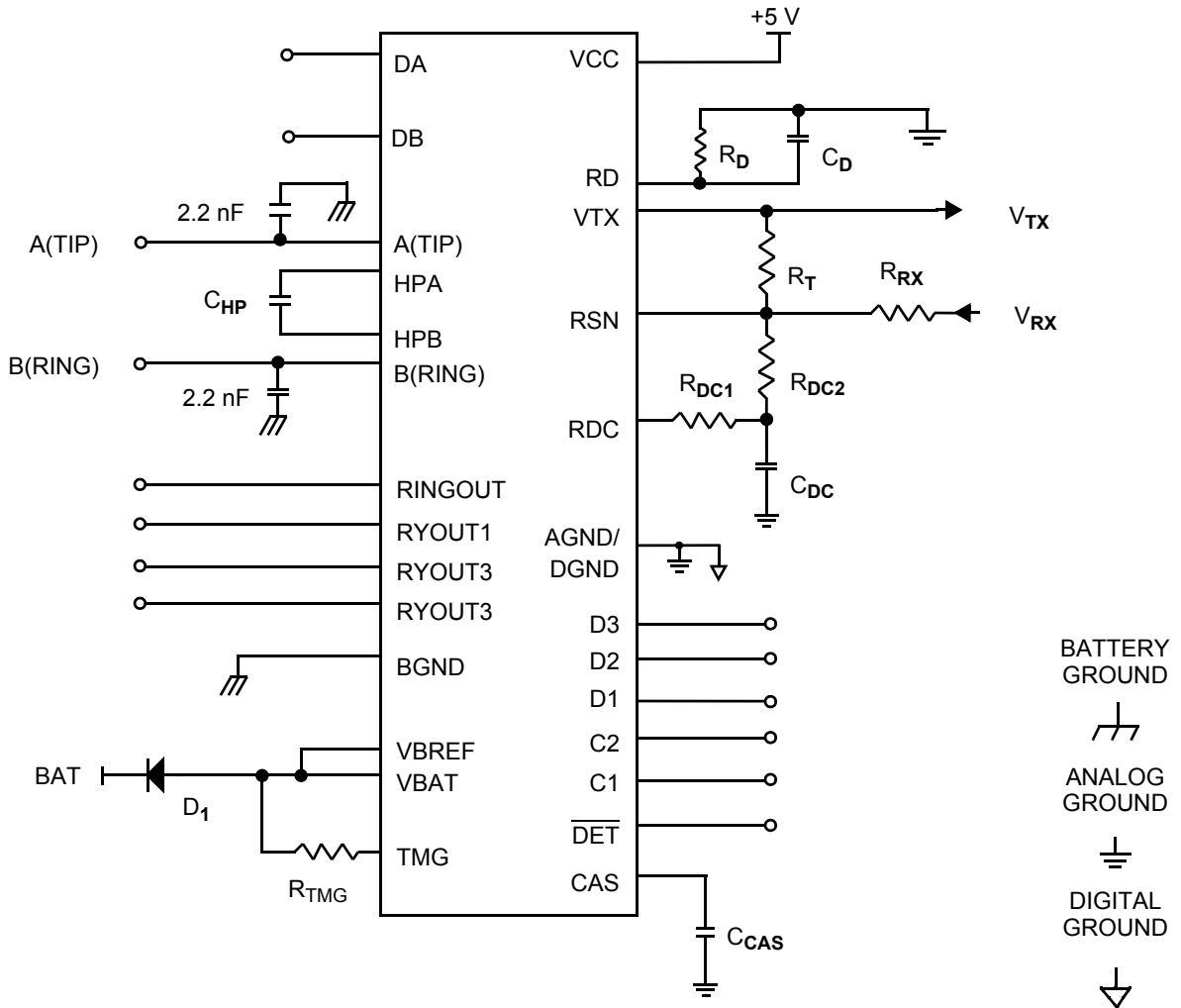
**Figure 1. DC Feed Characteristics**

## TEST CIRCUITS

**A. Two- to Four-Wire Insertion Loss****B. Four- to Two-Wire Insertion Loss and Balance Return Signal****C. Longitudinal Balance**

**TEST CIRCUITS (continued)****D. Two-Wire Return Loss Test Circuit****E. Loop-Detector Switching****F. RFI Test Circuit**

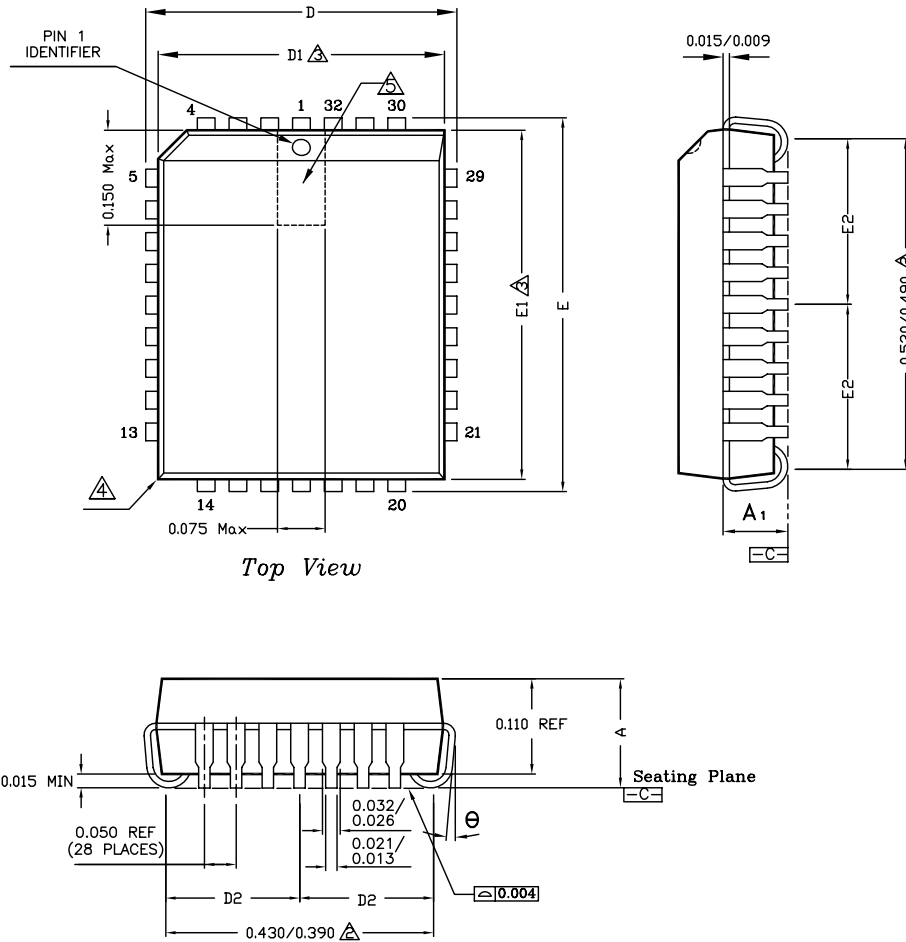
## TEST CIRCUITS (continued)



G. Le7920 Test Circuit

## PHYSICAL DIMENSIONS

## 32-Pin PLCC



## NOTES:

| 32-Pin PLCC    |           |       |        |
|----------------|-----------|-------|--------|
| JEDEC # MS-016 |           |       |        |
| Symbol         | Min       | Nom   | Max    |
| A              | 0.125     | --    | 0.140  |
| A1             | 0.075     | 0.090 | 0.095  |
| D              | 0.485     | 0.490 | 0.495  |
| D1             | 0.447     | 0.450 | 0.453  |
| D2             | 0.205 REF |       |        |
| E              | 0.585     | 0.590 | 0.595  |
| E1             | 0.547     | 0.550 | 0.553  |
| E2             | 0.255 REF |       |        |
| Θ              | 0 deg     | --    | 10 deg |

- 1 Dimensioning and tolerancing conform to ASME Y14.5M-1994.
- 2 To be measured at seating plan **- C -** contact point.
- 3 Dimensions "D1" and "E1" do not include mold protrusion. Allowable mold protrusion is 0.010 inch per side. Dimensions "D" and "E" include mold mismatch and determined at the parting line; that is "D1" and "E1" are measured at the extreme material condition at the upper or lower parting line.
- 4 Exact shape of this feature is optional.
- 5 Details of pin 1 identifier are optional but must be located within the zone indicated.
- 6 Sum of DAM bar protrusions to be 0.007 max per lead.
- 7 Controlling dimension : Inch.
- 8 Reference document : JEDEC MS-016

## 32-Pin PLCC

**Note:**

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

## REVISION SUMMARY

### Revision C to Revision D

- Minor changes were made to the datasheet style and format to conform to Zarlink standards.

### Revision D to Revision E

- Absolute Maximum Ratings: Added ESD immunity specification.

### Revision E to Revision F

- Added the 28-pin SOIC connection diagram and the SC option to the ordering information.

### Revision F to Revision G

- The physical dimension (PL032) was added to the Physical Dimension section.

### Revision G to Revision H

- Deleted the plastic DIP package and references to it.
- Updated the Pin Description table to correct inconsistencies.

### Revision H to Revision I

- Updated device name from "Am7920" to "Le7920" throughout document.
- Absolute Maximum Ratings: Notes updated to standard.
- Operating Ranges: Temperature statement updated to standard.
- Updated "Sales Office Listing."
- Updated physical dimension drawings.

### Revision I1 to Revision J1

- Added green package OPN to [Ordering Information, on page 3](#)
- Added [Package Assembly, on page 7](#)
- Updated 32-pin PLCC drawing in [Physical Dimensions, on page 17](#)
- Removed SOIC package information

### Revision J1 to Revision J2

- Enhanced format of package drawing in [Physical Dimensions, on page 17](#)
- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007



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